Physical Design of a Stacked Heterogeneous Multi-Core Processor

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Abstract: With the end of Dennard scaling, three dimensional stacking has emerged as a promising integration technique to improve microprocessor performance. In this talk, we present a physical design methodology for a stacked multi-core processor. We present the fast thread migration and cache-core decoupling features enabled by 3D chip stacking. We explain the various flows involved and present the lessons learned during the design process. The logic dies were fabricated with the Global Foundries 130 nm process and were stacked using the Ziptronix face-to-face (F2F) bonding technology. We also present a comparative analysis which highlights the benefits of 3D integration. Results indicate up to 18% reduction in total wire length and 25% lower critical path delay for critical inter-core components in the 3D implementation compared to 2D implementations.